

DIGITAL ELECTRONICS

BOOLEAN ALGEBRA

1. In boolean algebra, the OR operation is performed by which properties?

- a) Associative properties
- b) Commutative properties
- c) Distributive properties
- d) All of the Mentioned

Answer: d

Explanation: The expression for Associative property is given by $A+(B+C) = (A+B)+C$ & $A*(B*C) = (A*B)*C$.

The expression for Commutative property is given by $A+B = B+A$ & $A*B = B*A$.

The expression for Distributive property is given by $A+BC=(A+B)(A+C)$ & $A(B+C) = AB+AC$.

2. The expression for Absorption law is given by

- a) $A+AB = A$
- b) $A+AB = B$
- c) $AB+AA' = A$
- d) None of the Mentioned

Answer: a

Explanation: The expression for absorption law is given by $A+AB = A$.

3. According to boolean law: $A + 1 = ?$

- a) 1
- b) A
- c) 0
- d) A'

Answer: a

Explanation: $A + 1 = A$.

4. The involution of A is equal to

- a) A
- b) A'
- c) 1
- d) 0

Answer: a

Explanation: The involution of A means double inversion of A(i.e. A'') and is equal to A.

5. $A(A + B) = ?$

- a) AB
- b) 1
- c) $(1 + AB)$

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d) A

Answer: d

Explanation: $A(A + B) = AA + AB = A + AB = A(1 + B) = A \cdot 1 = A$.

6. DeMorgan's theorem states that

a) $(AB)' = A' + B'$

b) $(A + B)' = A' * B$

c) $A' + B' = A'B'$

d) None of the Mentioned

Answer: a

Explanation: The DeMorgan's law states that $(AB)' = A' + B'$ & $(A + B)' = A' * B'$.

7. $(A + B)(A' * B') = ?$

a) 1

b) 0

c) AB

d) AB'

Answer: b

Explanation: $(A + B)(A' * B') = AA'B' + BA'B' = 0 + BB'A' = 0 + 0 = 0$ ($AA' = BB' = 0$).

8. Complement of the expression $A'B + CD'$ is

a) $(A' + B)(C' + D)$

b) $(A + B')(C' + D)$

c) $(A' + B)(C' + D)$

d) $(A + B')(C + D')$

Answer: b

Explanation: $(A'B + CD')' = (A'B)'(CD')' = (A'' + B')(C' + D'') = (A + B')(C' + D)$.

9. Simplify $Y = AB' + (A' + B)C$

a) $AB' + C$

b) $AB + AC$

c) $A'B + AC'$

d) $AB + A$

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Answer: a

Explanation: $Y = AB' + (A' + B)C = AB' + (A' + B)C = AB' + (AB')'C = AB' + C$.

10. The boolean function $A + BC$ is a reduced form of

- a) $AB + BC$
- b) $(A + B)(A + C)$
- c) $A'B + AB'C$
- d) $(A + C)B$

Answer: b

Explanation: $(A + B)(A + C) = AA + AC + AB + BC = A + AC + AB + BC = A(1 + C + B) + BC = A + BC$.

ARITHMETIC OPERATIONS

1. What is the addition of the binary numbers 11011011010 and 010100101?

- a) 0111001000
- b) 1100110110
- c) 11101111111
- d) 10011010011

Answer: c

Explanation:

$$\begin{array}{r} 11011011010 \\ + 00010100101 \\ \hline 11101111111 \end{array}$$

2. Perform binary addition: $101101 + 011011 = ?$

- a) 011010
- b) 1010100
- c) 101110
- d) 1001000

Answer: d

Explanation:

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$$\begin{array}{r} 11111 \\ 101101 \\ +011011 \\ \hline 1001000 \\ \hline \end{array}$$

Therefore, the addition of $101101 + 011011 = 1001000$

3. Perform binary subtraction: $101111 - 010101 = ?$
- a) 100100
 - b) 010101
 - c) 011010
 - d) 011001

Answer: c

Explanation:

$$\begin{array}{r} 101111 \\ -010101 \\ \hline 011010 \\ \hline \end{array}$$

Therefore, The subtraction of $101111 - 010101 = 011010$

4. Binary subtraction of $100101 - 011110$ is
- a) 000111
 - b) 111000
 - c) 010101
 - d) 101010

Answer: a

Explanation:

$$\begin{array}{r} 100101 \\ -011110 \\ \hline 000111 \\ \hline \end{array}$$

Therefore, The subtraction of $100101 - 011110 = 000111$

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5. Perform multiplication of the binary numbers: $01001 \times 01011 = ?$

- a) 001100011
- b) 110011100
- c) 010100110
- d) 101010111

Answer: a

Explanation:

$$\begin{array}{r} 01001 \\ \times 01011 \\ \hline 01001 \\ 010010 \\ 0000000 \\ 01001000 \\ 000000000 \\ \hline 001100011 \\ \hline \end{array}$$

Therefore, $01001 \times 01011 = 001100011$

6. $100101 \times 0110 = ?$

- a) 1011001111
- b) 0100110011
- c) 101111110
- d) 0110100101

Answer: c

Explanation:

$$\begin{array}{r} 100101 \\ \times 0110 \\ \hline 000000 \\ 1001010 \\ 10010100 \\ 000000000 \\ \hline 011011110 \\ \hline \end{array}$$

Therefore, $100101 \times 0110 = 011011110$

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7. On multiplication of (10.10) and (01.01), we get

- a) 101.0010
- b) 0010.101
- c) 011.0010
- d) 110.0011

Answer: c

Explanation:

$$\begin{array}{r} 10.10 \\ \times 01.01 \\ \hline 1010 \\ 00000 \\ 101000 \\ 0000000 \\ \hline 011.0010 \end{array}$$

Therefore, $10.10 \times 01.01 = 011.0010$

8. Divide the binary numbers: $111101 \div 1001$ and find the remainder

- a) 0010
- b) 1010
- c) 1100
- d) 0011

Answer: d

Explanation:

$$\begin{array}{r} 1001 \overline{) 111101} (11 \\ \underline{1001} \\ 01100 \\ \underline{1001} \\ 0111 \end{array}$$

Therefore, the remainder of $111101 \div 1001 = 0111$

9. Divide the binary number (011010000) by (0101) and find the quotient

- a) 100011
- b) 101001

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- c) 110010
- d) 010001

Answer: b

Explanation:

0 1 0 1) 0 1 1 0 1 0 0 0 0 (1 0 1 0 0 1
0 1 0 1

0 0 0 1 1 0
0 1 0 1

0 0 1 0 0 0
0 1 0 1

0 1 1

Therefore, the quotient of $011010000 \div 1001 = 101001$

10. Binary subtraction of $101101 - 001011 = ?$

- a) 100010
- b) 010110
- c) 110101
- d) 101100

Answer: a

Explanation:

1 0 1 1 0 1
- 0 0 1 0 1 1

1 0 0 0 1 0

Therefore, the subtraction of $101101 - 001011 = 100010$

1's and 2's, 9's and 10's COMPLEMENT

1. 1's complement of 1011101 is

- a) 0101110
- b) 1001101
- c) 0100010
- d) 1100101

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Answer: c

Explanation: None.

2. 2's complement of 11001011 is

- a) 01010111
- b) 11010100
- c) 00110101
- d) 11100010

Answer: c

Explanation: None.

3. On subtracting $(01010)_2$ from $(11110)_2$ using 1's complement, we get

- a) 01001
- b) 11010
- c) 10101
- d) 10100

Answer: d

Explanation: None.

4. On subtracting $(010110)_2$ from $(1011001)_2$ using 2's complement, we get

- a) 0111001
- b) 1100101
- c) 0110110
- d) 1000011

Answer: d

Explanation: None.

5. On subtracting $(001100)_2$ from $(101001)_2$ using 2's complement, we get

- a) 1101100
- b) 011101
- c) 11010101
- d) 11010111

Answer: b

Explanation: None.

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6. On addition of 28 and 18 using 2's complement, we get

- a) 00101110
- b) 0101110
- c) 00101111
- d) 1001111

Answer: b

Explanation: None.

7. On addition of +38 and -20 using 2's complement, we get

- a) 11110001
- b) 100001110
- c) 010010
- d) 110101011

Answer: c

Explanation: None.

8. On addition of -46 and +28 using 2's complement, we get

- a) -10010
- b) -00101
- c) 01011
- d) 0100101

Answer: a

Explanation: None.

9. On addition of -33 and -40 using 2's complement, we get

- a) 1001110
- b) -110101
- c) 0110001
- d) -1001001

Answer: d

Explanation: None.

10. On subtracting +28 from +29 using 2's complement, we get

- a) 11111010
- b) 111111001
- c) 010101011

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d) 1

Answer: d

Explanation: None.

11. If the number of bits in the sum exceeds the number of bits in each added numbers, it results in

- a) Successor
- b) Overflow
- c) Underflow
- d) None of the Mentioned

Answer: b

Explanation: If the number of bits in the sum exceeds the number of bits in each added numbers, it results in overflow and is also known as excess-one.

12. An overflow is a

- a) Software problem
- b) Hardware problem
- c) User input problem
- d) None of the Mentioned

Answer: b

Explanation: An overflow is a hardware problem. It is not able to show correct result because of sign changes.

13. An overflow occurs in

- a) MSD position
- b) LSD position
- c) Middle position
- d) Never occurs

Answer: a

Explanation: An overflow occurs at Most Significant Digit position.

14. Logic circuitry is used to detect

- a) Underflow
- b) MSD
- c) Overflow

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d) LSD

Answer: c

Explanation: To check the overflow logic circuitry is used in each case.

15. 1's complement can be easily obtained by using

- a) Comparator
- b) Inverter
- c) Adder
- d) Subtractor

Answer: b

Explanation: With the help of inverter the 1's complement is easily obtained. Since, during the operation of 1's complement 1 is converted into 0 and vice-versa and this is well suited for the inverter.

16. The advantage of 2's complement system is that

- a) Only one arithmetic operation is required
- b) Two arithmetic operations are required
- c) No arithmetic operations are required
- d) None of the Mentioned

17. The 1's complements requires

- a) Two operations
- b) One operations
- c) Three operations
- d) None of the Mentioned

Answer: a

Explanation: Two operations are required for 1's complement operation. These are conversion of binary numbers and addition/subtraction.

18. Which one is used for logical manipulations ?

- a) 2's complement
- b) 9's complement
- c) 1's complement
- d) 10's complement

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Answer: c

Explanation: For logical manipulations 1's complement is used.

19. For arithmetic operations only

- a) 1's complement is used
- b) 2's complement
- c) 3's complement
- d) 9's complement

Answer: b

Explanation: Only 2's complement is used for arithmetic operations.

20. The addition of +19 and +43 results as _____ in 2's complement system.

- a) 11001010
- b) 101011010
- c) 00101010
- d) 00111110

Answer: d

Explanation: None.

LOGIC CIRCUITS

1. If the number of bits in the sum exceeds the number of bits in each added numbers, it results in

- a) Successor
- b) Overflow
- c) Underflow
- d) None of the Mentioned

Answer: b

Explanation: If the number of bits in the sum exceeds the number of bits in each added numbers, it results in overflow and is also known as excess-one.

2. An overflow is a

- a) Software problem
- b) Hardware problem
- c) User input problem
- d) None of the Mentioned

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Answer: b

Explanation: An overflow is a hardware problem. It is not able to show correct result because of sign changes.

3. An overflow occurs in
- a) MSD position
 - b) LSD position
 - c) Middle position
 - d) Never occurs

Answer: a

Explanation: An overflow occurs at Most Significant Digit position.

4. Logic circuitry is used to detect
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 - b) MSD
 - c) Overflow
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Explanation: To check the overflow logic circuitry is used in each case.

5. 1's complement can be easily obtained by using
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 - c) Adder
 - d) Subtractor

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Explanation: With the help of inverter the 1's complement is easily obtained. Since, during the operation of 1's complement 1 is converted into 0 and vice-versa and this is well suited for the inverter.

6. The advantage of 2's complement system is that
- a) Only one arithmetic operation is required
 - b) Two arithmetic operations are required
 - c) No arithmetic operations are required
 - d) None of the Mentioned

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Answer: a

Explanation: The advantage of 2's complement is that only one arithmetic operation is required for 2's complement's operation and that is either addition or subtraction.

7. The 1's complements requires

- a) Two operations
- b) One operations
- c) Three operations
- d) None of the Mentioned

Answer: a

Explanation: Two operations are required for 1's complement operation. These are conversion of binary numbers and addition/subtraction.

8. Which one is used for logical manipulations ?

- a) 2's complement
- b) 9's complement
- c) 1's complement
- d) 10's complement

Answer: c

Explanation: For logical manipulations 1's complement is used.

9. For arithmetic operations only

- a) 1's complement is used
- b) 2's complement
- c) 3's complement
- d) 9's complement

Answer: b

Explanation: Only 2's complement is used for arithmetic operations.

10. The addition of +19 and +43 results as _____ in 2's complement system.

- a) 11001010
- b) 101011010
- c) 00101010
- d) 00111110

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Answer: d

Explanation: None.

NUMBER SYSTEMS

1. Any signed negative binary number is recognised by its

- a) MSB
- b) LSB
- c) Bits
- d) Nibble

Answer: a

Explanation: Any negative number is recognized by its MSB(Most Significant Bit).

2. The parameter through which 16 distinct values can be represented is known as:

- a) Bit
- b) Byte
- c) Nibble
- d) Word

Answer: c

Explanation: It can be represented up to 16 different values with the help of Nibble. Though, Nibble is a combination of four bits and it takes four bits to represent a single BCD or hexadecimal digit.

3. If the decimal number is a fraction then its binary equivalent is obtained by_____the number continuously by 2.

- a) Dividing
- b) Multiplying
- c) Adding
- d) Subtracting

Answer: b

Explanation: On multiplying the decimal number continuously by 2, the binary equivalent is obtained.

4. The representation of octal number $(532.2)_8$ in decimal is :

- a) $(346.25)_{10}$

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- b) $(532.864)_{10}$
- c) $(340.67)_{10}$
- d) $(531.668)_{10}$

Answer: a

Explanation: $(532.2)_8 = 5 * 8^2 + 3 * 8^1 + 2 * 8^0 + 2 * 8^{-1} = (346.25)_{10}$

5. The decimal equivalent of the binary number $(1011.011)_2$ is

- a) $(11.375)_{10}$
- b) $(10.123)_{10}$
- c) $(11.175)_{10}$
- d) $(9.23)_{10}$

Answer: a

Explanation: $1 * 2^3 + 0 * 2^2 + 1 * 2^1 + 1 * 2^0 + 0 * 2^{-1} + 1 * 2^{-2} + 1 * 2^{-3} = (11.375)_{10}$

Hence, $(1011.011)_2 = (11.375)_{10}$

6. An important drawback of binary system is

- a) It requires very large string of 1's and 0's to represent a decimal number
- b) It requires sparingly small string of 1's and 0's to represent a decimal number
- c) It requires large string of 1's and small string of 0's to represent a decimal number
- d) None of the Mentioned

Answer: a

Explanation: The most vital drawback of binary system is that it requires very large string of 1's and 0's to represent a decimal number.

7. The decimal equivalent of the octal number $(645)_8$ is _____

- a) $(450)_{10}$
- b) $(451)_{10}$
- c) $(421)_{10}$
- d) $(501)_{10}$

Answer: c

Explanation: The decimal equivalent of the octal number $(645)_8$ is $6 * 8^2 + 4 * 8^1 + 5 * 8^0 = (421)_{10}$.

8. The largest two digit hexadecimal number is _____

- a) $(FE)_{16}$

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- b) (FD)₁₆
- c) (FF)₁₆
- d) (EF)₁₆

Answer: c

Explanation: The largest two digit hexadecimal number is (FF)₁₆.

9. Representation of hexadecimal number (6DE)₁₆ in decimal :

- a) $6 * 16^2 + 13 * 16^1 + 14 * 16^0$
- b) $6 * 16^2 + 12 * 16^1 + 13 * 16^0$
- c) $6 * 16^2 + 11 * 16^1 + 14 * 16^0$
- d) $6 * 16^2 + 14 * 16^1 + 15 * 16^0$

Answer: a

Explanation: In hexadecimal number D & E represents 13 & 14 respectively.

So, $6DE = 6 * 16^2 + 13 * 16^1 + 14 * 16^0$.

10. The quantity of double word is

- a) 16 bits
- b) 32 bits
- c) 64 bits
- d) 8 bits

Answer: b

Explanation: The quantity of double word is 32 bits.

11. The given hexadecimal number (1E.53)₁₆ is equivalent to

- a) (35.684)₈
- b) (36.246)₈
- c) (34.340)₈
- d) (35.599)₈

Answer: b

Explanation: $(1E.53)_{16} = (0001\ 1110.0101\ 0011)_2$
 $= (00011110.01010011)_2$
 $= (011110.010100110)_2$
 $= (011\ 110.010\ 100\ 110)_2$
 $= (36.246)_8$

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12. The octal number $(651.124)_8$ is equivalent to _____

- a) $(1A9.2A)_{16}$
- b) $(1B0.10)_{16}$
- c) $(1A8.A3)_{16}$
- d) $(1B0.B0)_{16}$

Answer: a

Explanation: $(651.124)_8 = (110\ 101\ 001.001\ 010\ 100)_2$
 $= (110101001.001010100)_2$
 $= (0001\ 1010\ 1001.0010\ 1010)_2$
 $= (1A9.2A)_{16}$

13. The octal equivalent of the decimal number $(417)_{10}$ is _____

- a) $(641)_8$
- b) $(619)_8$
- c) $(640)_8$
- d) $(598)_8$

Answer: a

Explanation: $8 \mid 417$
 $8 \mid 52 - 1$
 $8 \mid 6 - 4$
So, $(417)_{10} = (641)_8$

14. Convert the hexadecimal number $(1E2)_{16}$ to decimal:

- a) 480
- b) 483
- c) 482
- d) 484

Answer: c

Explanation: $(1E2)_{16} = 1 * 16^2 + 14 * 16^1 + 2 * 16^0$ (Since, E = 14)
 $= 256 + 224 + 2 = (482)_{10}$

15. $(170)_{10}$ is equivalent to

- a) $(FD)_{16}$
- b) $(DF)_{16}$
- c) $(AA)_{16}$
- d) $(AF)_{16}$

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Answer: c

Explanation: $16 \mid 170$

$16 \mid 10 - 10$

Hence, $(170)_{10} = (AA)_{16}$

16. Convert $(214)_8$ into decimal:

a) $(140)_{10}$

b) $(141)_{10}$

c) $(142)_{10}$

d) $(130)_{10}$

Answer: a

Explanation: $(214)_8 = 2 * 8^2 + 1 * 8^1 + 4 * 8^0$
 $= 128 + 8 + 4 = (140)_{10}$

17. Convert $(0.345)_{10}$ into an octal number:

a) $(0.16050)_8$

b) $(0.26050)_8$

c) $(0.19450)_8$

d) $(0.24040)_8$

Answer: b

Explanation: $0.345 * 8 = 2.762$

$0.760 * 8 = 6.086$

$0.08 * 8 = 0.640$

$0.640 * 8 = 5.125$

$0.120 * 8 = 0.960$

So, $(0.345)_{10} = (0.26050)_8$

18. Convert the binary number $(01011.1011)_2$ into decimal:

a) $(11.6875)_{10}$

b) $(11.5874)_{10}$

c) $(10.9876)_{10}$

d) $(10.7893)_{10}$

Answer: a

Explanation: $(01011)_2 = 0 * 2^4 + 1 * 2^3 + 0 * 2^2 + 1 * 2^1 + 1 * 2^0 = 11$

$(.1011)_2 = 1 * 2^{-1} + 0 * 2^{-2} + 1 * 2^{-3} + 1 * 2^{-4} = 0.6875$

So, $(01011.1011)_2 = (11.6875)_{10}$

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19. Octal to binary conversion: $(24)_8 = ?$

- a) $(111101)_2$
- b) $(010100)_2$
- c) $(111100)_2$
- d) $(101010)_2$

Answer: c

Explanation: $(24)_8 = (010100)_2$

20. Convert binary to octal: $(110110001010)_2 = ?$

- a) $(5512)_8$
- b) $(6612)_8$
- c) $(4532)_8$
- d) $(6745)_8$

Answer: b

Explanation: $(110110001010)_2 = (6612)_8$

SOP and POS

1. The logical sum of two or more logical product terms is called

- a) SOP
- b) POS
- c) OR operation
- d) NAND operation

Answer: a

Explanation: The logical sum of two or more logical product terms, is called SOP (i.e. sum of product).

2. The expression $Y=AB+BC+AC$ shows the _____ operation.

- a) EX-OR
- b) SOP
- c) POS
- d) NOR

Answer: b

Explanation: The given expression has the operation product as well as the sum of that. So, it shows SOP operation.

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3. The expression $Y=(A+B)(B+C)(C+A)$ shows the _____ operation.
- a) AND
 - b) POS
 - c) SOP
 - d) NAND

Answer: b

Explanation: The given expression has the operation sum as well as the product of that. So, it shows POS(product of sum) operation.

4. A product term containing all K variables of the function in either complemented or uncomplemented form is called a
- a) Minterm
 - b) Maxterm
 - c) Midterm
 - d) None of the Mentioned

Answer: a

Explanation: A product term containing all K variables of the function in either complemented or uncomplemented form is called a minterm.

5. According to the property of minterm, how many combination will have value equal to 1 for K input variables?
- a) 0
 - b) 1
 - c) 2
 - d) 3

Answer: b

Explanation: The main property of a minterm is that it possesses the value 1 for only one combination of K input variables and the remaining will have the value 0.

6. The canonical sum of product form of the function $y(A,B) = A + B$ is
- a) $AB + BB + A'A$
 - b) $AB + AB' + A'B$
 - c) $BA + BA' + A'B'$
 - d) None of the Mentioned

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Answer: b

Explanation: $A + B = A.1 + B.1 = A(B + B') + B(A + A') = AB + AB' + BA + BA' = AB + AB' + A'B + A'B'$

7. A variable on its own or in its complemented form is known as a

- a) Product Term
- b) Literal
- c) Sum Term
- d) None of the Mentioned

Answer: b

Explanation: A literal is a single logic variable or its complement. For example — X, Y, A', Z, X' etc.

8. Maxterm is the sum of _____ of the corresponding Minterm with its literal complemented.

- a) Terms
- b) Words
- c) Numbers
- d) None of the Mentioned

Answer: a

Explanation: Maxterm is the sum of terms of the corresponding Minterm with its literal complemented.

9. Canonical form is a unique way of representing _____

- a) SOP
- b) Minterm
- c) Boolean Expressions
- d) A page

Answer: c

Explanation: Boolean Expressions are represented through canonical form. An example of canonical form is $A'B'C' + AB'C + ABC'$.

10. There are _____ Minterms for 3 variables (a, b, c).

- a) 0
- b) 2
- c) 8
- d) None of the Mentioned

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Answer: c

Explanation: Minterm is given by 2^n . So, $2^3 = 8$ minterms are required.

11. _____ expressions can be implemented using either (1) 2-level AND-OR logic circuits or (2) 2-level NAND logic circuits.

- a) POS
- b) Literals
- c) SOP
- d) None of the Mentioned

Answer: c

Explanation: SOP expressions can be implemented using either (1) 2-level AND-OR logic circuits or (2) 2-level NAND logic circuits.

LOGIC GATES AND NETWORKS

1. A single transistor can be used to build which of the following digital logic gates?

- a) AND gates
- b) OR gates
- c) NOT gates
- d) NAND gates

Answer: c

Explanation: A transistor can be used as a switch. That is, when base is low collector is high (input zero, output one) and base is high collector is low (input 1, output 0).

2. How many truth table entries are necessary for a four-input circuit?

- a) 4
- b) 8
- c) 12
- d) 16

Answer: d

Explanation: For 2 inputs: $2^2 = 4$ truth table entries are necessary.

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3. Which input values will cause an AND logic gate to produce a HIGH output?

- a) At least one input is HIGH
- b) At least one input is LOW
- c) All inputs are HIGH
- d) All inputs are LOW

Answer: c

Explanation: For AND gate, the output is high only when both inputs are high. That's why the high output in AND will occur only when all the inputs are high.

4. Exclusive-OR (XOR) logic gates can be constructed from what other logic gates?

- a) OR gates only
- b) AND gates and NOT gates
- c) AND gates, OR gates, and NOT gates
- d) OR gates and NOT gates

Answer: c

Explanation: Expression for XOR is: $A.(B')+(A').B$
so in the above expression the following logic gates are used: AND, OR, NOT.

5. The basic logic gate whose output is the complement of the input is the:

- a) OR gate
- b) AND gate
- c) INVERTER gate
- d) Comparator

Answer: c

Explanation: It is also called NOT gate and it simply inverts the input.

6. The AND function can be used to _____ and the OR function can be used to

- a) Enable, disable
- b) Disable, enable
- c) Synchronize, energize
- d) Detect, invert

Answer: a

Explanation: Because of their multiplicity and additivity property respectively.

DIGITAL ELECTRONICS

7. The dependency notation " ≥ 1 " inside a block stands for which operation?

- a) OR
- b) XOR
- c) AND
- d) XNOR

Answer: a

Explanation: The dependency notation " ≥ 1 " inside a block stands for OR operation.

8. If we use an AND gate to inhibit a signal from passing one of the inputs must be

- a) LOW
- b) HIGH
- c) Inverted
- d) Floating

Answer: a

Explanation: AND gate means $A*B$ and OR gate means $A+B$ and to inhibit means to get low signal, one of the input must be low. It means ($0*1=0$ or $1*0=0$) we will get low output signal.

9. Logic gate circuits contain predictable gate functions that open theirs

- a) Outputs
- b) Inputs
- c) Pre-state
- d) None of the Mentioned

Answer: b

Explanation: Logic gate circuits contain predictable gate functions that open their inputs because we are free to give any types of inputs.

10. How many NAND circuits are contained in a 7400 NAND IC?

- a) 1
- b) 2
- c) 4
- d) 8

Answer: c

Explanation: 7400 IC's pin has total 14 pin. Pin no 7 use for GND and pin no 14 used for +vcc and remaining pins used for connections. For a NAND gate two inputs are required and one output is obtained means for NAND gate 3 pin connections are required.

DIGITAL ELECTRONICS

KARNAUGH MAP

1. A Karnaugh map (K-map) is an abstract form of _____ diagram organized as a matrix of squares.

- a) Venn Diagram
- b) Cycle Diagram
- c) Block diagram
- d) Triangular Diagram

Answer: a

Explanation: A Karnaugh map (K-map) is an abstract form of Venn diagram organized as a matrix of squares.

2. There are _____ cells in a 4-variable K-map.

- a) 12
- b) 16
- c) 18
- d) None of the Mentioned

Answer: b

Explanation: There are $16(2^4)$ cells in a 4-variable K-map.

3. The K-map based Boolean reduction is based on the following Unifying Theorem: $A + A' = 1$.

- a) Impact
- b) Non Impact
- c) Force
- d) None of the Mentioned

Answer: b

Explanation: The given expression $A + A' = 1$ is based on non-impact unifying theorem.

4. Each product term of a group, $w'.x.y'$ and $w.y$, represents the _____ in that group.

- a) Input
- b) POS
- c) Sum-of-Minterms
- d) None of the Mentioned

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Answer: c

Explanation: In a minterm, each variable w, x or y appears once either as the variable itself or as the inverse. So, the given expression satisfies the property of Sum of Minterm.

5. The prime implicant which has at least one element that is not present in any other implicant is known as

- a) Essential Prime Implicant
- b) Implicant
- c) Complement
- d) None of the Mentioned

Answer: a

Explanation: Essential prime implicants are prime implicants that cover an output of the function that no combination of other prime implicants is able to cover.

6. Product-of-Sums expressions can be implemented using

- a) 2-level OR-AND logic circuits
- b) 2-level NOR logic circuits
- c) 2-level XOR logic circuits
- d) Both 2-level OR-AND and NOR logic circuits

Answer: d

Explanation: Product-of-Sums expressions can be implemented using 2-level OR-AND & NOR logic circuits.

7. Each group of adjacent Minterms (group size in powers of twos) corresponds to a possible product term of the given

- a) Function
- b) Value
- c) Set
- d) None of the Mentioned

Answer: a

Explanation: Each group of adjacent Minterms (group size in powers of twos) corresponds to a possible product term of the given function.

8. Don't care conditions can be used for simplifying Boolean expressions in

- a) Examples
- b) Terms
- c) K-maps

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d) Latches

Answer: c

Explanation: Don't care conditions can be used for simplifying Boolean expressions in K-maps which helps in pairing with 1/0.

9. It should be kept in mind that don't care terms should be used along with the terms that are present in

- a) Minterms
- b) Maxterm
- c) K-Map
- d) Latches

Answer: a

Explanation: It should be kept in mind that don't care terms should be used along with the terms that are present in minterms which reduces the complexity of the boolean expression.

10. Using the transformation method you can realize any POS realization of OR-AND with only.

- a) XOR
- b) NAND
- c) AND
- d) NOR

Answer: d

Explanation: Using the transformation method we can realize any POS realization of OR-AND with only NOR.

11. There are many situations in logic design in which simplification of logic expression is possible in terms of XOR and _____ operations.

- a) X-NOR
- b) XOR
- c) NOR
- d) NAND

Answer: a

Explanation: There are many situations in logic design in which simplification of logic expression is possible in terms of XOR and XNOR operations.

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12. These logic gates are widely used in _____ design and therefore are available in IC form.

- a) Circuit
- b) Digital
- c) Analog
- d) Block

13. In case of XOR/XNOR simplification we have to look for the following _____

- a) Diagonal Adjacencies
- b) Offset Adjacencies
- c) Straight Adjacencies
- d) Both diagonal and offset adjencies

Answer: d

Explanation: In case of XOR/XNOR simplification we have to look for the following diagonal and offset adjacencies.

14. Entries known as _____ mapping.

- a) Diagonal
- b) Straight
- c) K
- d) None of the Mentioned

Answer: a

Explanation: Entries known as diagonal mapping.

K-MAP SIMPLIFICATION

1. Which statement below best describes a Karnaugh map?

- a) It is simply a rearranged truth table
- b) The Karnaugh map eliminates the need for using NAND and NOR gates
- c) Variable complements can be eliminated by using Karnaugh maps
- d) A Karnaugh map can be used to replace Boolean rules

Answer: a

Explanation: K-map is simply a rearranged truth table.

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2. Which of the examples below expresses the commutative law of multiplication?

- a) $A + B = B + A$
- b) $A \cdot B = B + A$
- c) $A \cdot (B \cdot C) = (A \cdot B) \cdot C$
- d) $A \cdot B = B \cdot A$

Answer: d

Explanation: The cumulative law of multiplication is $(A * B) = (B * A)$.

3. The Boolean expression $Y = (AB)'$ is logically equivalent to what single gate?

- a) NAND
- b) NOR
- c) AND
- d) OR

Answer: a

Explanation: If A and B are the input for AND gate the output is obtained as AB and after inversion we get $(AB)'$, which is the expression of NAND gate.

4. The observation that a bubbled input OR gate is interchangeable with a bubbled output AND gate is referred to as:

- a) A Karnaugh map
- b) DeMorgan's second theorem
- c) The commutative law of addition
- d) The associative law of multiplication

Answer: b

Explanation: DeMorgan's Law: $\sim(P \wedge Q) \Leftrightarrow \sim P \vee \sim Q$
 $\sim(P \vee Q) \Leftrightarrow \sim P \wedge \sim Q$.

5. The systematic reduction of logic circuits is accomplished by:

- a) Symbolic reduction
- b) TTL logic
- c) Using Boolean algebra
- d) Using a truth table

Answer: c

Explanation: The systematic reduction of logic circuits is accomplished by using boolean algebra.

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6. Each “1” entry in a K-map square represents:

- a) A HIGH for each input truth table condition that produces a HIGH output
- b) A HIGH output on the truth table for all LOW input combinations
- c) A LOW output for all possible HIGH input conditions
- d) A DON'T CARE condition for all possible input truth table combinations

Answer: a

Explanation: Each “1” entry in a K-map square represents a HIGH for each input truth table condition that produces a HIGH output.

7. Each “0” entry in a K-map square represents:

- a) A HIGH for each input truth table condition that produces a HIGH output
- b) A HIGH output on the truth table for all LOW input combinations
- c) A LOW output for all possible HIGH input conditions
- d) A DON'T CARE condition for all possible input truth table combinations

Answer: a

Explanation: Each “0” entry in a K-map square represents a LOW output for all possible HIGH input conditions.

8. Which of the following statements accurately represents the two BEST methods of logic circuit simplification?

- a) Boolean algebra and Karnaugh mapping
- b) Karnaugh mapping and circuit waveform analysis
- c) Actual circuit trial and error evaluation and waveform analysis
- d) Boolean algebra and actual circuit trial and error evaluation

Answer: c

Explanation: The two BEST methods of logic circuit simplification Boolean algebra and Karnaugh mapping.

9. Looping on a K-map always results in the elimination of

- a) Variables within the loop that appear only in their complemented form
- b) Variables that remain unchanged within the loop
- c) Variables within the loop that appear in both complemented and uncomplemented form
- d) Variables within the loop that appear only in their uncomplemented form

Answer: c

Explanation: Looping on a K-map always results in the elimination of variables within the loop that appear in both complemented and uncomplemented form.

DIGITAL ELECTRONICS

10. Which of the following expressions is in the sum-of-products form?

- a) $(A + B)(C + D)$
- b) $(A * B)(C * D)$
- c) $A * B *(CD)$
- d) $A * B + C * D$

Answer: d

Explanation: Sum of product means that the number is multiplied firstly and then it is added: $A * B + C * D$.

11. Which of the following is an important feature of the sum-of-products form of expressions?

- a) All logic circuits are reduced to nothing more than simple AND and OR operations
- b) The delay times are greatly reduced over other forms
- c) No signal must pass through more than two gates, not including inverters
- d) The maximum number of gates that any signal must pass through is reduced by a factor of two

Answer: a

Explanation: An important feature of the sum-of-products form of expressions in the given option is that all logic circuits are reduced to nothing more than simple AND and OR operations.

12. Which of the following expressions is in the product-of-sums form?

- a) $(A + B)(C + D)$
- b) $(AB)(CD)$
- c) $AB(CD)$
- d) $AB + CD$

Answer:

Explanation: $(A + B)(C + D)$ represents the product-of-sums form.

QUINE-MC CLUSKEY OR TABULATION METHOD

1. The output of an EX-NOR gate is 1. Which input combination is correct?

- a) $A = 1, B = 0$
- b) $A = 0, B = 1$
- c) $A = 0, B = 0$
- d) None of the Mentioned

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Answer: c

Explanation: The output of EX-NOR gate is given by $(AB' + A'B)'$. So, for $A = 0$ and $B = 0$ the output will be 1.

2. In which of the following gates the output is 1 if and only if at least one input is 1?

- a) AND
- b) NOR
- c) NAND
- d) OR

Answer: d

Explanation: In or gate we need at least one bit to be equal to 1 to generate the output as 1 because OR means any of the condition out of two is equal to 1 which means if at least one input is 1 then it shows output as 1.

3. The time required for a gate or inverter to change its state is called

- a) Rise time
- b) Decay time
- c) Propagation time
- d) Charging time

Answer: c

Explanation: The time required for a gate or inverter to change its state is called propagation time.

4. What is the minimum number of two input NAND gates used to perform the function of two input OR gates?

- a) One
- b) Two
- c) Three
- d) Four

Answer: c

Explanation: $Y = A + B$. This is the equation of OR gate. We require 3 NAND gates to create OR gate. We can also write,

1st, 2nd and 3rd NAND operations as: $Y = (A \text{ AND } B)' = A.B = (A.B)'$.

5. Odd parity of word can be conveniently tested by

- a) OR gate
- b) AND gate
- c) NAND gate

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d) XOR gate

Answer: d

Explanation: Odd parity of word can be conveniently tested by XOR gate.

6. The number of full and half adders are required to add 16-bit number is

- a) 8 half adders, 8 full adders
- b) 1 half adders, 15 full adders
- c) 16 half adders, 0 full adders
- d) 4 half adders, 12 full adders

Answer: b

Explanation: One half adder can add the least significant bit of the two numbers whereas full adders are required to add the remaining 15 bits as they all involve adding carries.

7. Which of the following will give the sum of full adders as output?

- a) Three point major circuit
- b) Three bit parity checker
- c) Three bit comparator
- d) Three bit counter

Answer: d

Explanation: Three bit counter will give the sum of full adders as output.

8. Which of the following gate is known as coincidence detector?

- a) AND gate
- b) OR gate
- c) NOR gate
- d) NAND gate

9. An OR gate can be imagined as

- a) Switches connected in series
- b) Switches connected in parallel
- c) MOS transistor connected in series
- d) None of the mentioned

Answer: b

Explanation: OR gate means addition of two inputs, due to this reason it is imagined as switches connected in parallel.

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10. How many full adders are required to construct an m-bit parallel adder?

- a) $m/2$
- b) m
- c) $m-1$
- d) $m+1$

Answer: c

Explanation: We need adder for every bit. So we should need m bit adders. A full adder adds a carry bit to two inputs and produces an output and a carry. But the most significant bits can use a half adder which differs from the full adder as in that it has no carry input, so we need m-1 full adders in m bit parallel adder.

BINARY CODED DECIMAL

1. Binary coded decimal is a combination of

- a) Two binary digits
- b) Three binary digits
- c) Four binary digits
- d) None of the Mentioned

Answer: c

Explanation: Binary coded decimal is a combination of 4 binary digits. For example-8421.

2. The decimal number 10 is represented in its BCD form as

- a) 1010
- b) 01010
- c) 00010000
- d) 001010

Answer: c

Explanation: The decimal number 10 is represented in its BCD form as 0001 0000.

3. Add the two BCD numbers: $1001 + 0100 = ?$

- a) 1101
- b) 00001101
- c) 00110011

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d) None of the mentioned

Answer: c

Explanation: Firstly, Add the 1001 and 0100. We get 1101 as output but it's not in BCD form. So, we add 0110 (i.e. 6) with 1101. As a result we get 10011 and it's BCD form is 0001 0011.

4. Carry out BCD subtraction for (68) – (61) using 10's complement method.

- a) 00000111
- b) 01110000
- c) 100000111
- d) 011111000

Answer: a

Explanation: None.

5. Code is a symbolic representation of _____ information.

- a) Continuous
- b) Discrete
- c) binary
- d) None of the Mentioned

Answer: b

Explanation: Code is a symbolic representation of discrete information, which may be present in the form of numbers, letters or physical quantities.

6. When numbers, letters or words are represented by a special group of symbols, this process is called

- a) Decoding
- b) Encoding
- c) Coding
- d) None of the Mentioned

Answer: b

Explanation: When numbers, letters or words are represented by a special group of symbols, this process is called encoding. Encoding in the sense of fetching the codes or words in a computer.

7. A three digit decimal number requires _____ for representation in the conventional BCD format.

- a) 3 bits
- b) 6 bits

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- c) 12 bits
- d) 24 bits

Answer: c

Explanation: The number of bits needed to represent a given decimal number is always greater than the number of bits required for a straight binary encoding of the same. Hence, a three digit decimal number requires 12 bits for representation in BCD format.

8. How many bits would be required to encode decimal numbers 0 to 9999 in straight binary codes.
- a) 12
 - b) 14
 - c) 16
 - d) 18

Answer: c

Explanation: Total number of decimals to be represented = 10000 = $10^4 = 2^{13.29}$. Therefore, the number of bits required for straight binary encoding = 14.

9. The excess-3 code for 597 is given by
- a) 100011001010
 - b) 100010100111
 - c) 010110010111
 - d) 010110101101

Answer: a

Explanation: The addition of '3' to each digit yields the three new digits '8', '12' and '10'. Hence, the corresponding four-bit binary equivalents are 100011001010.

10. The decimal equivalent of the excess-3 number 110010100011.01110101 is
- a) 970.42
 - b) 1253.75
 - c) 861.75
 - d) None of the Mentioned

Answer: a

Explanation: The conversion of binary numbers into digits '1100', '1010', '0011', '0111' and '0101' gives '12', '5', '3', '7' and '5' respectively. Hence, the decimal number is 970.42.

DIGITAL ELECTRONICS

PROCEDURE FOR DESIGN OF COMBINATIONAL CIRCUITS

1. The basic building blocks of the arithmetic unit in a digital computers are

- a) Subtractors
- b) Adders
- c) Multiplexer
- d) None of the Mentioned

Answer: b

Explanation: The basic building blocks of the arithmetic unit in a digital computers are adders. Since, a parallel adder is constructed with a number of full-adder circuits connected in cascade. By controlling the data inputs to the parallel adder, it is possible to obtain different types of arithmetic operations.

2. A digital system consists of _____ types of circuits.

- a) 2
- b) 3
- c) 4
- d) 5

Answer: a

Explanation: A digital system consists of two types of circuits and these are combinational and sequential logic circuit.

3. In a combinational circuit, the output at any time depends only on the _____ at that time.

- a) Voltage
- b) Intermediate values
- c) Input values
- d) None of the Mentioned

Answer: c

Explanation: In a combinational circuit, the output at any time depends only on the input values at that time.

4. In a sequential circuit, the output at any time depends only on the input values at that time.

- a) Past output values
- b) Intermediate values
- c) Present input values

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d) None of the Mentioned

Answer: c

Explanation: In a sequential circuit, the output at any time depends on the present input values as well as past output values.

5. Procedure for the design of combinational circuits are:

- A. From the word description of the problem, identify the inputs and outputs and draw a block diagram.
 - B. Draw the truth table such that it completely describes the operation of the circuit for different combinations of inputs.
 - C. Simplify the switching expression(s) for the output(s).
 - D. Implement the simplified expression using logic gates.
 - E. Write down the switching expression(s) for the output(s).
- a) B, C, D, E, A
 - b) A, D, E, B, C
 - c) A, B, E, C, D
 - d) None of the Mentioned

Answer: c

Explanation: The given arrangement in option c is the right sequence for the designing of the combinational circuits.

6. All logic operations can be obtained by means of

- a) AND and NAND operations
- b) OR and NOR operations
- c) OR and NOT operations
- d) AND, OR and NOT operations

Answer: d

Explanation: Since, the logic gates AND, OR and NOT are called as universal logic gates. It means that any operations can be obtained by implementation of these gates.

7. The design of an ALU is based on

- a) Sequential logic
- b) Combinational logic
- c) Multiplexing
- d) None of the Mentioned

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Answer: b

Explanation: The design of an ALU is based on combinational logic. Because the unit has a regular pattern, it can be broken into identical stages connected in cascade through carries.

8. If the two numbers are unsigned, the bit conditions of interest are the _____ carry and a possible _____ result.

- a) Input, zero
- b) Output, one
- c) Input, one
- d) Output, zero

Answer: d

Explanation: If the two numbers are unsigned, the bit conditions of interest are the output carry and a possible zero result.

9. If the two numbers include a sign bit in the highest order position, the bit conditions of interest are the sign of the result, a zero indication and

- a) An underflow condition
- b) A neutral condition
- c) An overflow condition
- d) None of the Mentioned

Answer: c

Explanation: If the two numbers include a sign bit in the highest order position, the bit conditions of interest are the sign of the result, a zero indication and an overflow condition.

10. The flag bits in an ALU is defined as

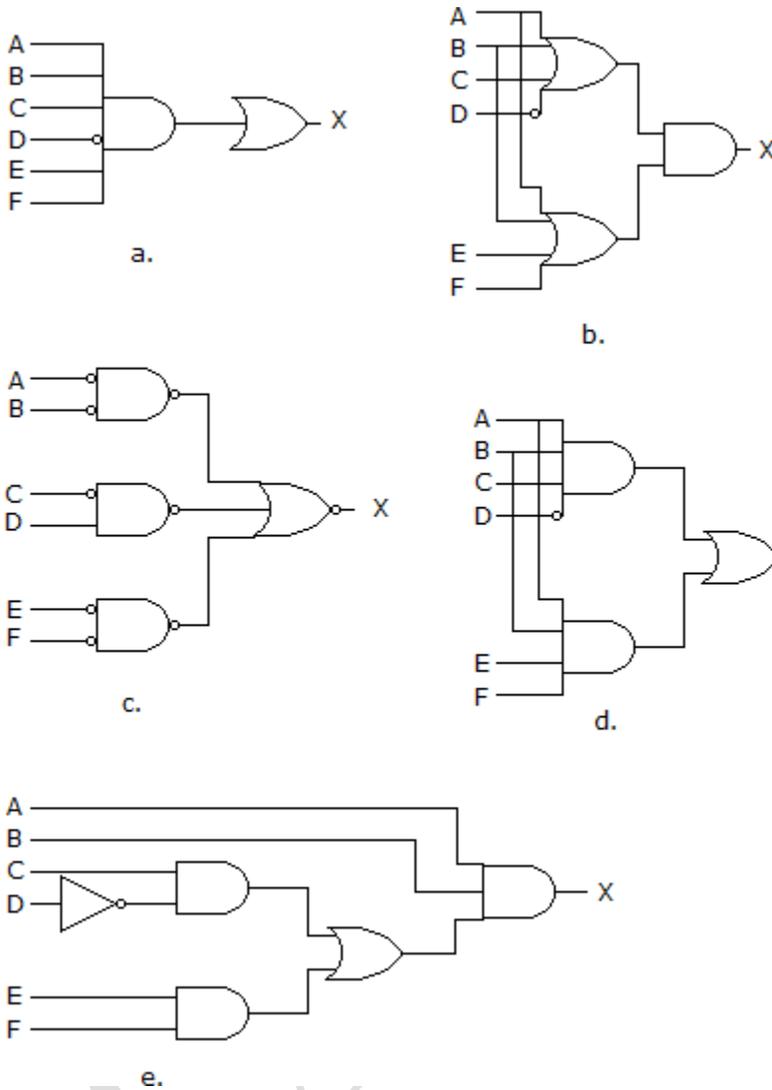
- a) The total number of registers
- b) The status bit conditions
- c) The total number of control lines
- d) All of the Mentioned

Answer: b

Explanation: In an ALU, status bit conditions are sometimes called condition code bits or flag bits.

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1. Which of the circuits in figure (a to d) is the sum-of-products implementation of figure (e)?



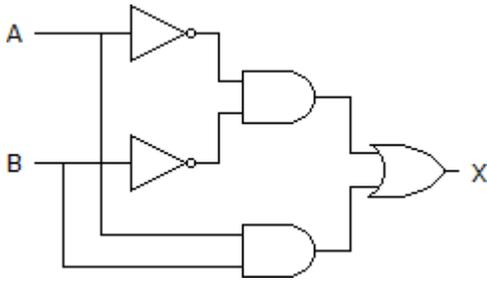
- a) a
- b) b
- c) c
- d) d

Answer: d

Explanation: Here, the diagram of option d contains the OR gate followed by the AND gates, so it is in SOP form.

2. Which of the following logic expressions represents the logic diagram shown?

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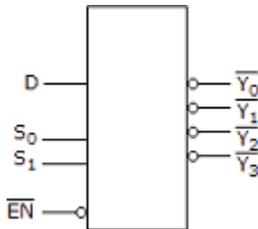


- a) $X=AB'+A'B$
- b) $X=(AB)'+AB$
- c) $X=(AB)'+A'B'$
- d) $X=A'B'+AB$

Answer: d

Explanation: 1st output of AND gate is $= A'B'$
2nd AND gate's output is $= AB$ and,
OR gate's output is $= (A'B')+(AB) = AB + A'B'$.

2. The device shown here is most likely a _____



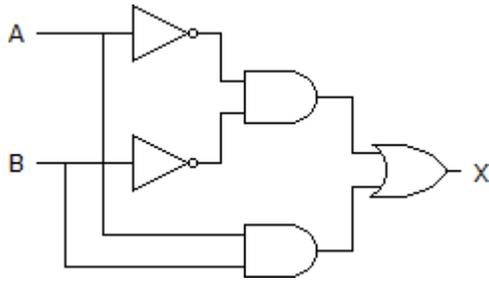
- a) Comparator
- b) Multiplexer
- c) Inverter
- d) Demultiplexer

Answer: d

Explanation: The given diagram is demultiplexer, because it takes single input & gives many outputs.

4. What type of logic circuit is represented by the figure shown below?

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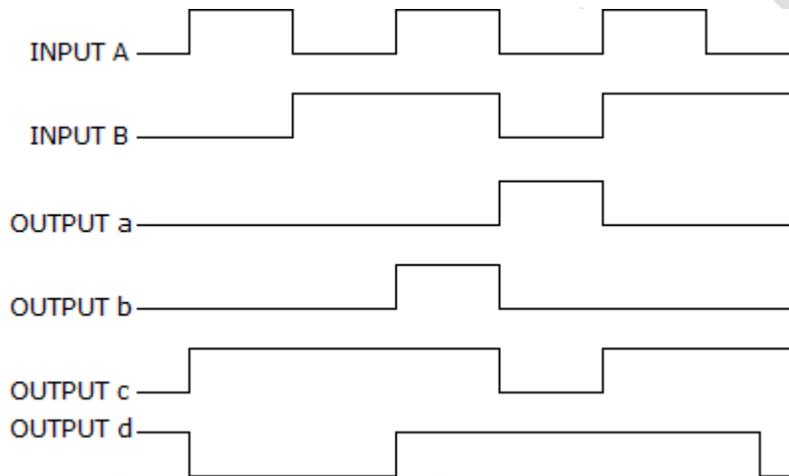


- a) XOR
- b) XNOR
- c) AND
- d) XAND

Answer: b

Explanation: After solving the circuit we get $(AB)' + AB$ as output, which is XNOR operation.

5. For a two-input XNOR gate, with the input waveforms as shown below, which output waveform is correct?



- a) d
- b) a
- c) c
- d) b

Answer: a

Explanation: When both inputs are same then the o/p is high for a XNOR gate.

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i.e., A B O/P

0 0 1

0 1 0

1 0 0

1 1 1.

6. Which of the following combinations of logic gates can decode binary 1101?

- a) One 4-input AND gate
- b) One 4-input AND gate, one inverter
- c) One 4-input AND gate, one OR gate
- d) One 4-input NAND gate, one inverter

Answer: b

Explanation: For decoding any number output must be high for that code and this is possible in D option only.

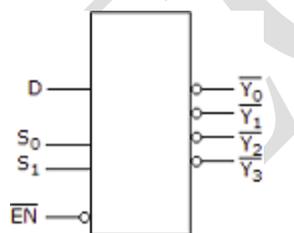
7. What is the indication of a short to ground in the output of a driving gate?

- a) Only the output of the defective gate is affected
- b) There is a signal loss to all load gates
- c) The node may be stuck in either the HIGH or the LOW state
- d) The affected node will be stuck in the HIGH state

Answer: b

Explanation: Short to ground in the output of a driving gate indicates of a signal loss to all load gates.

8. For the device shown here, assume the D input is LOW, both S inputs are LOW and the input is LOW. What is the status of the Y' outputs?



- a) All are HIGH
- b) All are LOW
- c) All but are LOW

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d) All but are HIGH

Answer: d

Explanation: In the given diagram, S0 and S1 are selection bits. So,

I/P S0 S1 O/P

D = 0 0 0 Y0

D = 0 0 1 Y1

D = 0 1 0 Y2

D = 0 1 1 Y3

Hence, inputs are S0 and S1 are Low means 0, so output is Y0.

9. The carry propagation can be expressed as _____

- a) $C_p = AB$
- b) $C_p = A + B$
- c) $C_p = A \text{ XOR } B$
- d) $C_p = A + B'$

Answer: b

Explanation: This happens in parallel adders (where we try to add numbers in parallel via more than one adders). A carry propagation occurs when carry from one adder needs to be forwarded to other adder and that second adder is holding the computation (addition) because carry from first adder has not come yet. So, there is a slight delay for second adder and this is known as carry propagation.

10. 3 bits full adder contains

- a) 3 combinational inputs
- b) 4 combinational inputs
- c) 6 combinational inputs
- d) 8 combinational inputs

Answer: d

Explanation: Three bits full adder requires $2^3 = 8$ combinational circuits.

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HALF ADDER and FULL ADDER

1. In parts of the processor, adders are used to calculate
- a) Addresses
 - b) Table indices
 - c) Increment and decrement operators
 - d) All of the Mentioned

Answer: d

Explanation: In parts of the processor, adders are used to calculate addresses, table indices, increment and decrement operators, and similar operations.

2. Total number of inputs in a half adder is
- a) 2
 - b) 3
 - c) 4
 - d) 1

Answer: a

Explanation: Total number of inputs in a half adder is two. Since, an EXOR gates has 2 inputs and carry is connected with the input of EXOR gates.

3. In which operation carry is obtained?
- a) Subtraction
 - b) Addition
 - c) Multiplication
 - d) Both addition and subtraction

Answer: b

Explanation: In addition, carry is obtained. For example: $1\ 0\ 1 + 1\ 1\ 1 = 1\ 0\ 0$; in this example carry is obtained after 1st addition (i.e. $1 + 1 = 1\ 0$).

4. If A and B are the inputs of a half adder, the sum is given by
- a) A AND B
 - b) A OR B
 - c) A XOR B
 - d) A EXOR B

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Answer: c

Explanation: If A and B are the inputs of a half adder, the sum is given by $A \oplus B$.

5. If A and B are the inputs of a half adder, the carry is given by

- a) $A \text{ AND } B$
- b) $A \text{ OR } B$
- c) $A \oplus B$
- d) $A \text{ EXOR } B$

Answer: a

Explanation: If A and B are the inputs of a half adder, the carry is given by: $A \text{ (AND) } B$.

6. Half-adders have a major limitation in that they cannot

- a) Accept a carry bit from a present stage
- b) Accept a carry bit from a next stage
- c) Accept a carry bit from a previous stage
- d) None of the Mentioned

Answer: c

Explanation: Half-adders have a major limitation in that they cannot accept a carry bit from a previous stage, meaning that they cannot be chained together to add multi-bit numbers. However, the two output bits of a half-adder can also represent the result $A+B=3$ as sum and carry both being high.

7. The difference between half adder and full adder is

- a) Half adder has two inputs while full adder has four inputs
- b) Half adder has one output while full adder has two outputs
- c) Half adder has two inputs while full adder has three inputs
- d) All of the Mentioned

Answer: c

Explanation: Half adder has two inputs while full adder has three inputs; this is the difference between them.

8. If A, B and C are the inputs of a full adder then the sum is given by

- a) $A \text{ AND } B \text{ AND } C$
- b) $A \text{ OR } B \text{ AND } C$
- c) $A \text{ OR } B \text{ OR } C$
- d) $A \oplus B \oplus C$

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Answer: c

Explanation: If A, B and C are the inputs of a full adder then the sum is given by A OR B OR C.

9. If A, B and C are the inputs of a full adder then the carry is given by

- a) A AND B OR (A OR B) AND C
- b) A OR B OR (A AND B) C
- c) (A AND B) OR (A AND B)C
- d) A XOR B XOR (A XOR B) AND C

Answer: a

Explanation: If A, B and C are the inputs of a full adder then the carry is given by A AND B OR (A OR B) AND C.

10. How many AND, OR and EXOR gates are required for the configuration of full adder

- a) 1, 2, 2
- b) 2, 1, 2
- c) 3, 1, 2
- d) 4, 0, 1

Answer: b

Explanation: There are 2 AND, 1 OR and 2 EXOR gates required for the configuration of full adder.

HALF SUBTRACTOR and FULL SUBTRACTOR

1. Half subtractor is used to perform subtraction of

- a) 2 bits
- b) 3 bits
- c) 4 bits
- d) 5 bits

Answer: a

Explanation: Half subtractor is a combinational circuit which is used to perform subtraction of two bits, namely minuend and subtrahend.

2. For subtracting 1 from 0, we use to take a _____ from neighbouring bits.

- a) Carry
- b) Borrow
- c) Not possible

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d) None of the Mentioned

Answer: b

Explanation: For subtracting 1 from 0, we use to take a borrow from neighbouring bits because carry is taken into consideration during addition process.

3. How many outputs are required for the implementation of a subtractor?

- a) 1
- b) 2
- c) 3
- d) 4

Answer: b

Explanation: There are two outputs required for the implementation of a subtractor. One for the output and another for borrow.

4. Let the input of a subtractor is A and B then what the output will be if $A = B$?

- a) 0
- b) 1
- c) A
- d) B

Answer: a

Explanation: The output for $A = B$ will be 0. If $A = B$, it means that $A = B = 0$ or $A = B = 1$. In both of the situation subtractor gives 0 as the output.

5. Let A and B is the input of a subtractor then the output will be

- a) A XOR B
- b) A AND B
- c) A OR B
- d) A EXNOR B

Answer: a

Explanation: Since, the output of a subtractor is given by $AB' + BA'$ and this is the output of a XOR gate. So, the final output is $AB' + BA'$.

6. Let A and B is the input of a subtractor then the borrow will be

- a) $A * B'$
- b) $A' * B$
- c) A OR B

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d) A AND B

Answer: b

Explanation: The borrow of a subtractor is received through NAND gate whose one input is inverted. On that basis the borrow will be $(A' * B)$.

7. What does minuend and subtrahend denotes in a subtractor?

- a) Their corresponding bits of input
- b) Its outputs
- c) Its inputs
- d) None of the Mentioned

Answer: c

Explanation: Minuend and subtrahend are the two bits of input of a subtractor. If A and B are the two inputs of a subtractor then A is called minuend and B as subtrahend.

8. Full subtractor is used to perform subtraction of

- a) 2 bits
- b) 3 bits
- c) 4 bits
- d) 8 bits

Answer: b

Explanation: Full subtractor is used to perform subtraction of 3 bits, namely minuend bit, subtrahend bit and borrow from the previous stage.

9. The full subtractor can be implemented using

- a) Two XOR and an OR gates
- b) Two half subtractors and an OR gate
- c) Two multiplexers and an AND gate
- d) None of the Mentioned

Answer: b

Explanation: The full subtractor can be implemented using two half subtractors and an OR gate.

10. The output of a subtractor is given by (if A, B and X are the inputs)

- a) A AND B XOR X
- b) A XOR B XOR X
- c) A OR B NOR X

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d) $A \text{ NOR } B \text{ XOR } X$

Answer: b

Explanation: The output of a subtractor is given by (if A, B and X are the inputs) $A \text{ XOR } B \text{ XOR } X$.

11. The output of a full subtractor is same as

- a) Half adder
- b) Full adder
- c) Half subtractor
- d) None of the Mentioned

Answer: b

Explanation: The output of a full adder and a full subtractor are same. If A, B and C are the input of a full adder and a full subtractor then the output will be given by $(A \text{ XOR } B \text{ XOR } C)$.